Claims

1. A noise removing circuit, comprising:

a highpass filter detecting a noise component included in an input signal;

a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said highpass filter becomes a predetermined reference voltage or higher;

an analog delaying circuit delaying the input signal by a predetermined amount of time, and outputting the delayed signal; and

an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse generated by said pulse generating circuit is input, and outputting the signal output from said analog delaying circuit unchanged in other cases, wherein said analog delaying circuit comprises

a plurality of capacitors,

a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to the

plurality of capacitors in a predetermined order at different timing, and

a plurality of second switches extracting the voltage of the input signal respectively held by said plurality of capacitors before next timing when the voltage is held is reached.

2. A noise removing circuit, comprising:

a noise extracting circuit extracting a noise component included in an input signal;

a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher;

an analog delaying circuit having

a plurality of capacitors,

a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing, and

a plurality of second switches making said plurality of capacitors output the voltage of the input

signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit; and

an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and outputting the signal output from said analog delaying circuit unchanged in other cases.

3. A noise removing circuit, comprising:

a noise extracting circuit extracting a noise component included in an input signal;

a pulse generating circuit generating a pulse having a predetermined width at timing when a voltage level of the noise component output from said noise extracting circuit becomes a predetermined reference voltage or higher;

an analog delaying circuit having

a plurality of capacitors,

a plurality of first switches making said plurality of capacitors respectively hold the voltage of the input signal in correspondence with supply timing

by respectively supplying the input signal to said plurality of capacitors in a predetermined order at different timing, and

a plurality of second switches making said plurality of capacitors output the voltage of the input signal respectively held by said plurality of capacitors in a predetermined order at timing delayed by a predetermined amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit; and

an outputting circuit holding the signal output from said analog delaying circuit at immediately preceding timing when the pulse having the predetermined width is output from said pulse generating circuit, and outputting the signal output from said analog delaying circuit unchanged in other cases, wherein

all of said circuits are formed on a same semiconductor substrate with a MOS process.

4. The noise removing circuit according to claim 1, 2, or 3, wherein

output terminals of said plurality of second switches are connected in common.

5. The noise removing circuit according to any

of claims 1 to 4, wherein

said plurality of first switches are exclusively made electrically continuous.

6. The noise removing circuit according to any of claims 1 to 5, wherein

said plurality of second switches are exclusively made electrically continuous.

7. The noise removing circuit according to any of claims 1 to 6, wherein

each of said pluralities of first and second switches is an analog switch configured by connecting an FET of a p-channel type, and an FET of an n-channel type in parallel.

8. The noise removing circuit according to any of claims 1 to 7, wherein

said analog delaying circuit further comprises clock generating means for generating a clock signal that cyclically selects each of said plurality of first switches and said plurality of second switches.

9. The noise removing circuit according to claim 8, wherein

said clock generating means supplies a clock signal, whose one cycle is an amount of time required until when the pulse having the predetermined width is output from said pulse generating circuit, to said plurality of first switches and said plurality of second switches in a sequential order.

10. The noise removing circuit according to any of claims 1 to 8, wherein

said analog delaying circuit further comprises an output capacitor connected to each of said plurality of capacitors via said plurality of second switches.

11. The noise removing circuit according to claim 10, wherein

a capacitance of said output capacitor is set to a value smaller than a capacitance of each of said plurality of capacitors.

12. The noise removing circuit according to any of claims 1 to 10, wherein

constituent elements of the respective circuits are integrally formed on a semiconductor substrate.

13. The noise removing circuit according to any

of claims 1 to 10, wherein

constituent elements of the respective circuits are integrally formed on a same semiconductor substrate with a CMOS process.